

AMENDED CLAIM SET

1 1. (currently amended) A DRAM, comprising:

2 at least one primary sense amplifier, wherein the at least one primary sense
3 amplifier has single ended sensing, has data storage and data write-back capability, and
4 has at least two amplification stages; and

5 a plurality of storage cells and a plurality of bitlines, with a single ended bitline
6 structure, wherein ~~a~~ one storage cell of the plurality of storage cells and the at least one
7 primary sense amplifier are connected by ~~a~~ one single bitline of the plurality of bitlines;
8 wherein the DRAM has storage cells and bitlines.

1 2. (currently amended) The DRAM of claim 1, further comprising a plurality of
2 secondary sense amplifiers and a plurality of global bitlines, with a single ended global
3 bitline structure, wherein the at least one primary sense amplifier and ~~a~~ one secondary
4 sense amplifier of the plurality of secondary sense amplifiers are connected by ~~a~~ one
5 single global bitline of the plurality of global bitlines, ~~wherein the DRAM has secondary~~
6 ~~sense amplifiers and global bitlines.~~

1 3. (original) The DRAM of claim 2, wherein the DRAM further comprises a small
2 voltage swing design.

1 4. (currently amended) The DRAM of claim 2, wherein at least one of the plurality of
1 secondary sense amplifiers comprise at least two amplification stages.

1 5. (currently amended) The DRAM of claim 2, wherein the at least one primary sense
2 amplifier is being capable to decouple from the one single global bitline.

1 6. (original) The DRAM of claim 1, wherein the at least one primary sense amplifier
2 comprises MOS devices, and wherein at least one of the MOS devices has a customized
3 threshold.

1 7. (original) The DRAM of claim 6, wherein the customized threshold is dynamically
2 adjusted.

1 8. (original) The DRAM of claim 1, wherein the DRAM is an embedded DRAM.

1 9. (currently amended) A DRAM, comprising:

2 a single ended bitline structure, wherein the DRAM has bitlines;

3 a single ended global bitline structure, wherein the DRAM has global bitlines;

4 ~~a plurality of primary sense amplifiers operationally engaging the bitlines and the~~
5 ~~global bitlines, wherein the primary sense amplifiers have data storage and data write~~
6 ~~back capability, and wherein the primary sense amplifiers are being capable to decouple~~

1 from the global bitlines;

2 a full-wordline I/O structure[[.]] comprising a reduced address space, wherein the
3 reduced address space has no column address; wherein essentially all memory cell that
4 are simultaneously turned on by any one wordline are being operated on by associated
5 sense amplifiers of the primary sense amplifiers; wherein the DRAM has memory cells
6 and wordlines; and

7 a pipelined architecture, wherein the DRAM is functioning in cycles and in each
8 of the cycles an operation can be initiated, and wherein the pipelined architecture
9 comprise synchronized operations of the single ended bitline structure, of said single
10 ended global bitline structure, of the primary sense amplifiers, and of the full-wordline
11 I/O structure.

1 10. (canceled)

1 11. (currently amended) The DRAM of claim 9, wherein a Read command and a
2 subsequent WriteBack command of the commands are executed in differing cycles of the
3 cycles.

1 12. (currently amended) The DRAM of claim 9, wherein a Read command and a
2 subsequent WriteBack command of the commands are executed in a single one of the
3 cycles.

1 13. (canceled)

1 14. (currently amended) The DRAM of claim ~~13~~ 9, wherein a Read command and a Write
2 command ~~of the commands~~ are executed simultaneously in a single one of the cycles.

1 15. (original) The DRAM of claim 9, wherein a size of the DRAM can be increased in a
2 modular manner.

1 16. (original) The DRAM of claim 15, wherein the modular manner increase comprise an
2 I/O increase.

1 17. (original) The DRAM of claim 15, wherein the modular manner increase comprise a
2 banking increase.

1 18. (original) The DRAM of claim 9, wherein the DRAM further comprises a small
2 voltage swing design.

1 19. (canceled)

1 20. (original) The DRAM of claim 9, wherein the DRAM is an embedded DRAM.

1 21. (currently amended) A processor, comprising:

2 at least one embedded DRAM macro, wherein the at least one embedded DRAM
3 macro is further comprising:

4 a single ended bitline structure, wherein the DRAM has bitlines;

5 a single ended global bitline structure, wherein the DRAM has global bitlines;

6 ~~a plurality of primary sense amplifiers operationally engaging the bitlines and the~~
7 ~~global bitlines, wherein the primary sense amplifiers have data storage and data write-~~
8 ~~back capability, and wherein the primary sense amplifiers are being capable to decouple~~
9 ~~from the global bitlines;~~

10 a full-wordline I/O structure[[,]] comprising a reduced address space, wherein the
11 reduced address space has no column address; wherein essentially all memory cell that
12 are simultaneously turned on by any one wordline are being operated on by associated
13 sense amplifiers of the primary sense amplifiers, wherein the DRAM has memory cells
14 and wordlines; and

15 a pipelined architecture, wherein the DRAM is functioning in cycles and in each
16 of the cycles an operation can be initiated, and wherein the pipelined architecture
17 comprise synchronized operations of the single ended bitline structure, said single ended
18 global bitline structure, ~~the primary sense amplifiers;~~ and the full-wordline I/O structure.

1 22. (canceled)

1 23. (original) The processor of claim 21, wherein the DRAM further comprises a small
2 voltage swing design.